IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re The Application of:
David Chong Sook Lim et al.

Serial No.: 10/664,982

Filed: September 17, 2003

For: PACKAGING SYSTEM FOR DIE-UP CONNECTION OF A DIE-DOWN ORIENTED INTEGRATED CIRCUIT

Examiner: Leonardo Andujar

Art Unit: 2826

Cesari and McKenna, LLP
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December 30, 2008

Via EFS Web

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir

AMENDED APPEAL BRIEF under MPEP section 1205.03

This brief is being filed within one (1) months of the December 18, 2008 mailing date of the Notice of Non-Compliant Appeal Brief.

The first Appeal Brief filed January 29, 2008 was non-compliant due to omission of sections: (ix) Evidence Appendix and (x) Related Proceedings Appendix. This amended Brief contains those sections.

(i) Real party in Interest is Fairchild Semiconductor, Inc. of 82 Running Hill Rd., So. Portland, ME 04106.

(ii) There are no other appeals, interferences or judicial proceedings known that might affect or have a bearing on the Board's decision in this appeal.

(iii) Claims 1, 4, 5 and 8 are the only claims remaining in the case and all stand finally rejected under 35 USC 103(a).

Claims 2, 3, 6 and 7 are canceled.

(iv) No amendments have been filed subsequent to the final rejection.

(v) Summary of claimed subject matter involved in this appeal is found in all the claims that now exist in the application – claims 1, 4, 5 and 8.

Independent claim 1 reads as follows (the added **enbolded** letters reference the following comments):

INDEPENDENT CLAIM 1

1. A die containing package **(a)** comprising:

a die defining electrical die contacts, the die contacts arranged along a first and an opposite side of the die **(b)**,

a substrate defining first substrate contacts **(c),**

flattened electrical conductive balls **(d)** attached to the die contacts and making electrical connection thereto,

electrical conductive runs **(e)** on the substrate that run substantially under the die connecting the first substrate contacts, wherein the first substrate contacts are located adjacent to the first side of the die, to second substrate contacts, wherein the second substrate contacts are located adjacent to the opposite side of the die, electrically conductive wires **(f)** with first ends making electrical connections to the first substrate contacts, wherein the wires are formed to run substantially parallel to the surface of the die, and wherein the other ends are horizontally attached to the flattened balls.

Subject matter of claims being argued in section (vii).

(a) a die containing package - that is an integrated circuit package with a chip (die) mounted within the package; See prior art FIG. 1 for a die mounted "die up" in a package and FIG. 2 where a "die-down" mounting is shown. See pages 2 lines 15 to29.

(b) the die having electrical contacts along a first side and along the opposite side of the die. See page 5 lines 28 to 31.

(c) a substrate with first contacts – that is a substrate with electrical connection locations; See FIGs. 3, 4 and 5 the substrate 101 with the runs (traces) 102-107 the run (substantially) under the die. FIG. 4 shows the die 108 mounted onto the substrate shown in FIG. 5 which shows the runs (traces) running under (the dotted lines) the die 108. See page 4 lines 22 to page 5 line 31.

(d) flattened electrical conductive balls attached to and making electrical connections to the die contacts; See FIG. 7, item 218 are the flattened balls on the die 212.

(e) the electrical conductive runs on the substrate that make electrical connections between contacts adjacent to the first side of the die to contacts adjacent to the opposite side and the

die. For example see FIG. 3 where the die contact 110 connects to a wire 116 that connects to a run that passes under the die 108 an emerges on the substrate 122 opposite side of the die. FIG. 5 shows the substrate with the runs.

(f) electrically conductive wires are then connected from the substrate contacts to the flattened balls on the adjacent side of the die. See FIG. 7, the wire item 210 connected 222 to the substrate and 226 to the balls 218.

(g) See FIG. 7 wire 210 running parallel to the die 212 surface. And

(h) See FIG. 7 where the wire 217 attaches horizontally to the ball 220.

CLAIM 4 DEPENDS FROM CLAIM 1:

4. The die containing package of claim 1 wherein the second substrate contacts are located on the substrate to accommodate a pin out different from the die.

NOTE: Here the substance covered includes routing flexibility where the pin out may be altered. See page 6 lines 19 to 23.

INDEPENDENT CLAIM 5

5. A process for packaging (a) a die comprising the steps of:

defining electrical die contacts, the electrical die contacts arranged along a first and an opposite side of the die (b),

defining a substrate with first substrate contacts (c),

flattening electrical conductive balls (d),

attaching the flattened electrically conductive balls to the die contacts (d),

forming electrical conductive runs (e) on the substrate that run substantially under the die connecting the first substrate contacts, wherein the first substrate contacts are located adjacent to the first side of the die, to second substrate contacts, wherein the second substrate contacts are located adjacent to the opposite side of the die,

connecting electrically conductive wires (f) to the first substrate contacts,

running the electrically conductive wires substantially (g) parallel to the surface of the die to the die contacts, and

horizontally attaching the other ends of the wires to the flattened electrical conductive balls thereby making electrical connections there between, and wherein the other ends remain substantially parallel to the surface of the die (h).

NOTE: the reference letters in parentheses apply to both Claim 1 and claim 5.

CLAIM 8 DEPENDS FROM CLAIM 5:

8. The process of claim 5 further comprising the step of locating the second substrate contacts on the substrate to accommodate a pin out different from the die.

NOTE: Here the substance covered includes routing flexibility where the pin out may be altered. See page 6 lines 19 to 23.

(vi) Grounds for rejection that are to be reviewed on appeal

The Office Action of August 10, 2007 rejected claims 1, 4, 5 and 8 (all the claims remaining in this application) under 35 U.S.C. 103(a) as being unpatentable over Shim et al. (US 6,531,784) , hereafter "Shim," in view of Kang et al. (US 2003/017810 A1), hereafter "Kang.".

A specific language limitation/element of claims 1 and 5 and thus also in dependent claims 4 and 8 reads as follows:

> "...electrical conductive runs on the substrate that run substantially under the die connecting the first substrate contacts, wherein the first substrate contacts are located adjacent to the first side of the die, to second substrate contacts, wherein the second substrate contacts are located adjacent to the opposite side of the die..."

On page 2 of the office action (Appendix C), in paragraph 4, the Examiner cites Shim FIGs. 9 and 5 (Shim is attached as appendix B) as showing a die containing package

comprising a die 14 (FIG. 9) with electrical contacts item 34 (FIG. 5) arranged along the sides of the die. The Examiner continues (arguably referencing FIG. 9) as follows:

"...electrical contact runs 24 on the substrate that run substantially under the die connecting the first substrate contacts, wherein the first substrate contacts are located adjacent to the first side of the die, to second substrate contacts 22, wherein the second substrate contacts are located adjacent to the opposite side of the die..." Underlining added.

Review is requested of subject matter of the Examiner's above statement and the conclusions drawn there from. The above statement is a mis-read of Shim and is erroneous.

(vii) Argument (for all claims 1, 4, 5 and 8).

Argument is presented in two parts, the first part a) illustrates the Examiner's misunderstanding of Shim, noting that Shim does not disclosure or suggest structure or process to support the Examiner's findings; and b) a brief discussion of the present invention being Unobvious.

a) Shim in column 3. lines 48 et seq. states, "...conductive layers 22, 24 of a metal ...that comprises the top and bottom surface of the substrate... (they) are typically patterned...to define terminal pads 26...and solder ball lands 28 in the bottom layer."

Item 22 and 24 are metal **layers**, 22 is not a second substrate contact and 22 and 24 are **not runs.** The layers 22 and 24 **could** be etched into runs under the die, but **Shim does not disclose or suggest** runs on layers 22 and 24 that under the die from side to side!

See Shim's FIG. 1 where all the leads from the chip 14 connect 26 to a substrate 12 and to vias 30 through to solder balls 18. Please note **that none of the runs travel under the die 14 to contacts adjacent to the other side of the die**, as the claim limitation requires. Note that all the contacts shown for the IC's 14 and 16 (See FIGs. 1-3) are connected to pads 26 and to runs that DO NOT travel under the die.

With respect to FIG. 9 (and to all the other FIGs. in Shim), which was cited by the Examiner, please note that the layers 22 (shown as interrupted) and 24 are physically under the chip (as are other layers), but Shim does not show, discuss, suggest, or offer any reason or problem to be solved or advantage gained in forming runs under the dies 14 or 16.

FIGs. 7, 8 and 9 show solder balls beneath the dies 14 and 16. In these FIGs. there are no labels or discussion on the solder balls and vias shown in the middle of the FIGs. 7-9. **None** of the vias are shown as connecting the balls beneath the ICs and there is no discussion of runs. See FIGs. 2 or 3 where the ball 18 connects to a land 28 and to vias 30 to opening in the solder mask 32 for the pads 26 and the solder ball lands 28. Please note there is no such comparable structure shown for the interrupted layer 22, the unmarked vias and balls that are shown under the ICs (marked as B on page 3 of the attached Office Action, Appendix C). Notice that there can be no connections from the ICs 14 and 16 to

the top layer 22 that is under the ICs, as there is a break (marked as A on FIG. 9 in the Office Action) where the layer marked 22 IS NOT continuous under the dies and is not marked 22 under the dies and is not discussed under the dies. No connections can be made directly to the interrupted layer 22 under the dies.

On page 6 of the Office Action, Appendix C, the Examiner acknowledges the above argument and continues saying, "...Nonetheless, Shim (e.g., fig. 9) shows electrical conductive runs 24 on the substrate that run substantially under the die connecting the first and the second substrate contacts 22. Note the contacts 22 are connected by vias or plated through holes..."

The Examiner refers to item 22 as "contacts" whereas 22 is a metal layer, and the Examiner refers to item 24 as "conductive runs" whereas 24 is another metal layer. In fact **Shim only shows runs on FIG. 1** connecting pads 26 to vias 30. The runs are not marked, and these runs DO NOT TRAVEL UNDER THE DIE, in fact there is no discussion of runs at all. The metal layers 22 and 24 could be etched to produce runs, however, the only ones shown (and even those are not discussed) are those on FIG. 1, and there is no further mentions of runs discussed or shown, much less discussed or shown running under the die from one side to the other. Applicant's Attorney (below) remains puzzled and dismayed by these findings of the Examiner after these many years, many filings, amendments and responses to distinguish many references, a recent restriction, not to mention the expense to Fairchild.

One possible explanation for these unreferenced balls is shown in FIG. 11 where an IC pattern is shown with contacts around the entire periphery. An end view (as in FIGs. 7-9) would show the balls that are connected to leads at the far other end of the chip. From any angle solder balls would be shown even though none are connected under the ICs.

b) With respect to Obviousness, a person of ordinary skill in the applicable art would understand that etched runs may be formed on substrates mounting ICs. They, however, would not know that a manufacturer would be able to discontinue an IC package by allowing the pin out of a die-down type chip, mounted to the inventive substrate, to provide the pin out of a die-up chip. This chip/substrate combination can then be mounted in a die-up IC package, and the die-down IC package discontinued.

Finally, what advantage does this invention afford to Fairchild?

The title of this application is "Packaging System for Die-up Connection of a Die-Down Oriented Integrated Circuit." The fist sentence in the SUMMARY of the originally filed application reads as follows, "It is an object of the present invention to provide a packaging arrangement that would permit the connection of a die-down chip in a die-up configuration." The last sentence on Page 5 of the original application reads as follows, "More Generally (sic), the present invention is directed to arranging traces and wire contacts so that a die-down die may be packaged in a die-up orientation." This function is echoed throughout the application and the intervening actions on the application over the years.

Fairchild maintained two IC packaging systems, illustrated in FIGs. 1 and 2 in the original application, one for a die-up die and a second for a die-down die. With the introduction of the present invention the die-down die may be mounted on a substrate that reverses the pin-out from one side of the die to the other. This presents the die-down contacts on the opposite side (a mirror image) of the die in the same orientation that a die-up IC would present. The connections allow the die-down IC mounted to the substrate to be packaged in the die-up package without the wires crossing each other and causing shorts.

This invention allows Fairchild to discontinue the die-down package entirely thereby providing considerable saving for the corporation. See Appendix D, a Declaration by a Fairchild employee, Douglas Dolan, under 37 CFR 1.132. This is a copy of an affidavit filed by the undersigned attorney, Edwin H. Paul, on or about July 16, 2004 showing the unexpected benefit and commercial success of the present invention.

A number of discussions with the Examiner during the prosecution of this application proved fruitless.

Please charge any additional fee occasioned by this paper to our Deposit Account No. 03-1237.

Respectfully submitted,

/Edwin H. Paul/

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(viii) Claims Appendix

1. (previously presented) A die containing package comprising:

a die defining electrical die contacts, the die contacts arranged along a first and an opposite side of the die,

a substrate defining first substrate contacts,

flattened electrical conductive balls attached to the die contacts and making electrical connection thereto,

electrical conductive runs on the substrate that run substantially under the die connecting the first substrate contacts, wherein the first substrate contacts are located adjacent to the first side of the die, to second substrate contacts, wherein the second substrate contacts are located adjacent to the opposite side of the die, electrically conductive wires with first ends making electrical connections to the first substrate contacts, wherein the wires are formed to run substantially parallel to the surface of the die, and wherein the other ends are horizontally attached to the flattened balls.

2-3. canceled.

4. (previously presented) The die containing package of claim 1 wherein the second substrate contacts are located on the substrate to accommodate a pin out different from the die.

5. (previously presented) A process for packaging a die comprising the steps of:

defining electrical die contacts, the electrical die contacts arranged along a first and an opposite side of the die,

defining a substrate with first substrate contacts,

flattening electrical conductive balls,

attaching the flattened electrically conductive balls to the die contacts,

forming electrical conductive runs on the substrate that run substantially under the die connecting the first substrate contacts, wherein the first substrate contacts are located adjacent to the first side of the die, to second substrate contacts, wherein the second substrate contacts are located adjacent to the opposite side of the die,

connecting electrically conductive wires to the first substrate contacts,

running the electrically conductive wires substantially parallel to the surface of the die to the die contacts, and

horizontally attaching the other ends of the wires to the flattened electrical conductive balls thereby making electrical connections there between, and wherein the other ends remain substantially parallel to the surface of the die.

6-7. canceled.

8. (previously presented) The process of claim 5 further comprising the step of locating the second substrate contacts on the substrate to accommodate a pin out different from the die.

(ix) Evidence Appendix

a. U.S. Patent No. 6,531,784B1 to Shim et al. The patent copy is marked APPENDIX B. This patent was used by the Examiner in the present child application in the first Office Action dated 5/20/2005 and in the succeeding Office Actions.

b. Pages 2-8 of an Office Action dated 7/30/2007 from Examiner Andujar This paper is marked APPENDIX C.

c. A copy of a Declaration under 37 CFR 1.132 authored by Douglas Dolan a Fairchild Semiconductor Corp. employee. This Declaration is marked APPENDIX D.

This Declaration was filed in the parent case on July 16, 2004. The parent case is Application Serial No. 09/823,600, filed March 30, 2001. The parent application matured into U.S. Patent No. 6,891,257 B2 that issued May 10, 2005.

(x) Related Proceedings Appendix

NONE

APPENDIX D

PATENTS
112055-0040
17732-38560

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re The Application of: David Chong et al.	)	
Serial No.: 09/823,600	)	Examiner: Andujar, Leonardo
Filed: March 30, 2001	)	Art Unit: 2826
For: PACKAGING SYSTEM FOR DIE-UP CONNECTION OF A DIE-DOWN ORIENTED INTEGRATED CIRCUIT	)	

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CERTIFICATE OF TRANSMISSION

I hereby certify that the following paper is being facsimile transmitted to the Patent and Trademark Office on July 16, 2004.

_____
Edwin H. Paul

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

DECLARATION UNDER C.F.R. 1.132 OF DOUGLAS DOLAN

I, Douglas Dolan, being duly sworn do hereby state that I am an Employee of Fairchild Semiconductor corporation of South Portland, Maine, the owner of the above patent application.

My title is Patent Engineer, and I am intimately involved Fairchild's operations regarding intellectual property, in particular, patents and pending applications.

I am a member of the Patent Committee where decisions are made on applying for patents. These decisions have many aspects but most important are those inventions that promise, among other things, to decrease cost to manufacture. The present application is an important invention covering a product that is in high volume production and that is providing substantial savings for the company.

I am well aware of the present application and the product line directly affected by this application. I have retrieved some production quantity numbers that support the original decision to file for a patent. The decision to go forward with the present application was motivated by the prospects of eliminating an IC package type from our product line. In this particular case the economics of eliminating an IC package type at the cost of a substrate weighed heavily in favor of the substrate. This decision has been borne out in the market place and promises to have a greater effect in the near future.

To date the number of devices produced using the substrate cross over scheme that allows one IC package to accept either a die up die or a die down die mounted to the inventive substrate is approaching 200 million units. Moreover, we will produce about 200 million units this year with increases over the next four years of about 25% per year.

Needless to say, this is an important product and our competitive edge afforded by a patent covering this invention is very important. Our competitors continue to not realize the cost advantages of the invention.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 19 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

Sworn and ascribed to by Douglas Dolan

Respectfully submitted,_____ Date: _____

APPENDIX B

US006531784B1

(12) **United States Patent**
Shim et al.

(10) **Patent No.: US 6,531,784 B1**
(45) **Date of Patent: Mar. 11, 2003**

(54) **SEMICONDUCTOR PACKAGE WITH SPACER STRIPS**

(75) Inventors: **Il Kwon Shim**, Singapore (SG); **Kambhampati Ramakrishna**, Chandler, AZ (US); **Vincent DiCaprio**, Mesa, AZ (US)

(73) Assignee: **Amkor Technology, Inc.**, Chandler, AZ (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/585,915**

(22) Filed: **Jun. 2, 2000**

(51) **Int. Cl.**[7] **H01L 23/48**
(52) **U.S. Cl.** **257/777**; 257/779; 257/686; 257/780; 257/784
(58) **Field of Search** 257/668, 673, 257/686, 685, 693, 696, 703, 737, 738, 777, 780, 784, 779

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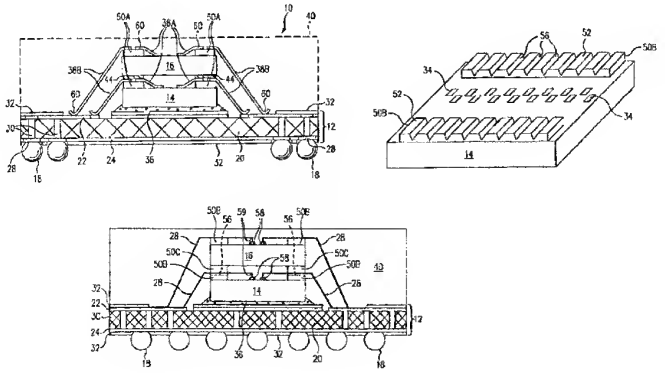
Primary Examiner—Albert W. Paladini
Assistant Examiner—Luan Thai
(74) *Attorney, Agent, or Firm*—Skjerven Morrill LLP; James E. Parsons

(57) **ABSTRACT**

A semiconductor package incorporates spacer strips enabling one or more semiconductor dies having central terminal pads to be stacked on top of one another within the package and reliably wire bonded to an associated substrate without shorting of the bonded wires. Each of the spacer strips comprises a flat, elongated strip of an insulative material that mount at edges of a surface of a die such that they straddle the central terminal pads thereon. The die is electrically connected to the substrate by a plurality of fine conductive wires having a first end bonded to one of the central terminal pad on the die, a second end bonded to a terminal pad on the substrate, and an intermediate portion between the first and second ends that passes transversely across the top surface of one of the spacer strips. The spacer strips have spaced pads or grooves on or in their top surfaces that captivate the individual wires and thereby redistribute the wires and prevent them from contacting the die and each other.

37 Claims, 5 Drawing Sheets



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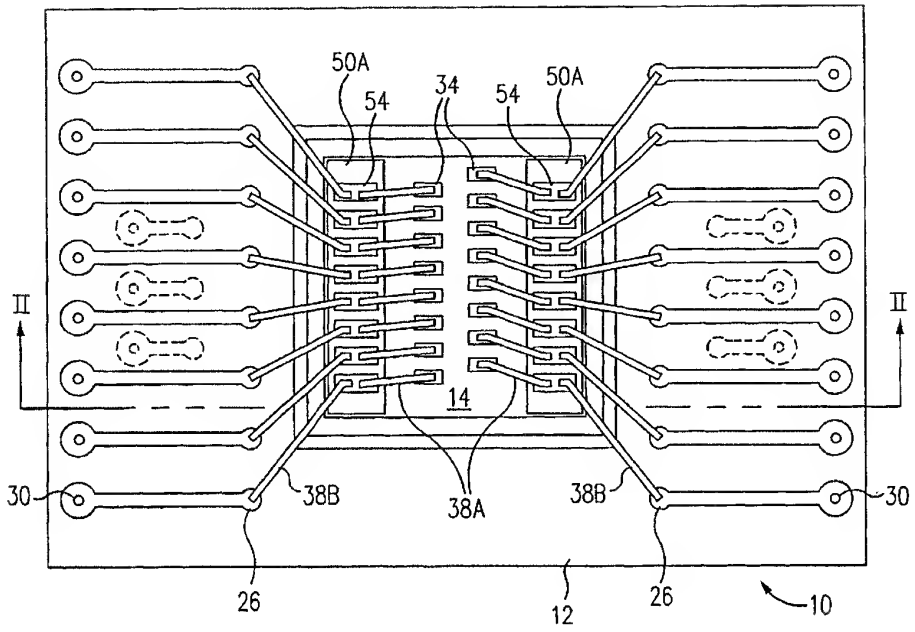
50A
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FIG. 1

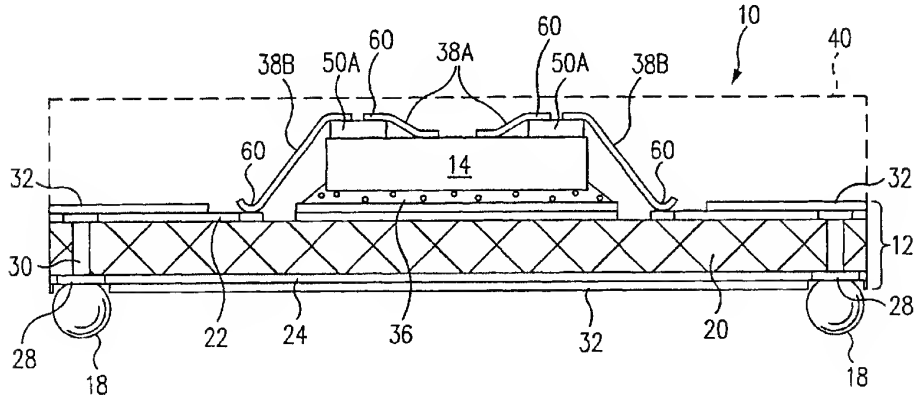
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FIG. 2

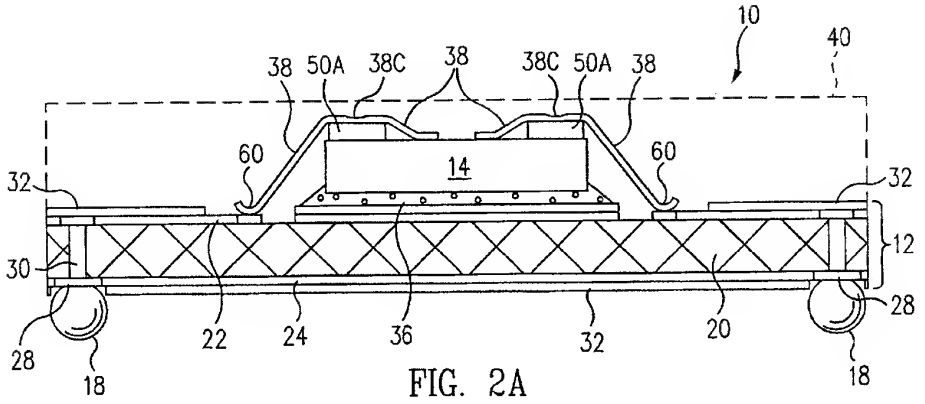


FIG. 2A

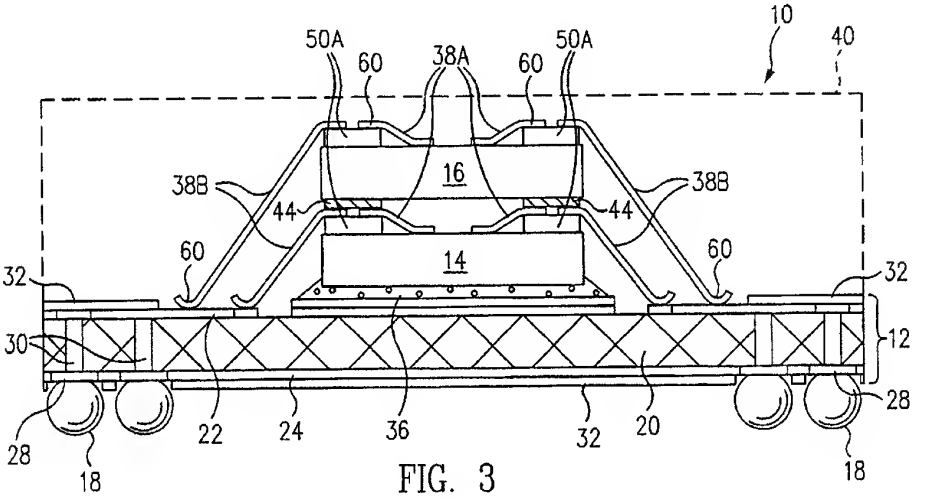


FIG. 3

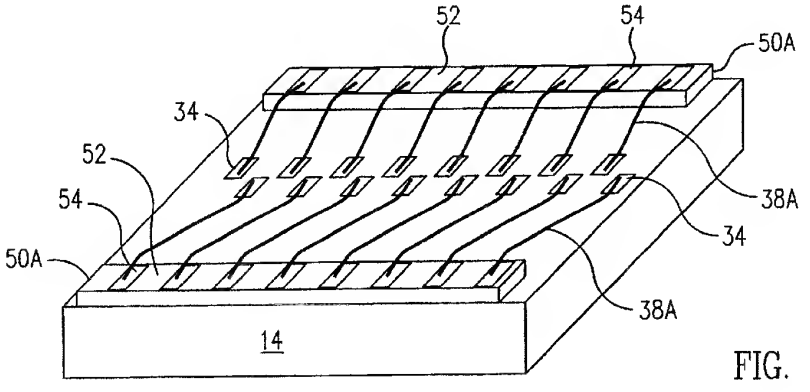


FIG. 4

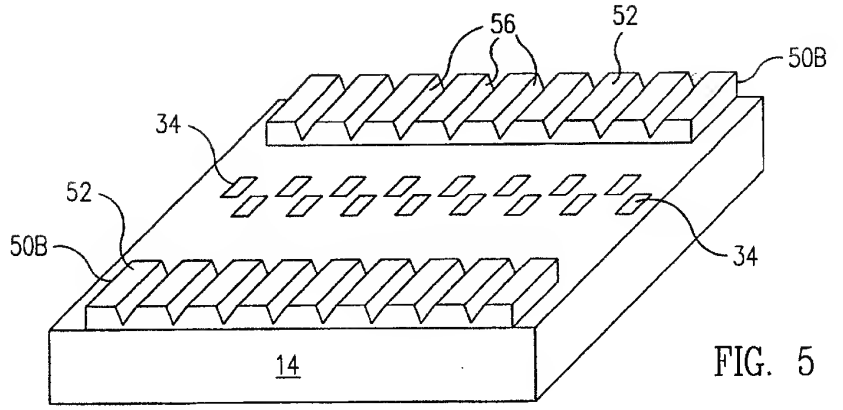


FIG. 5

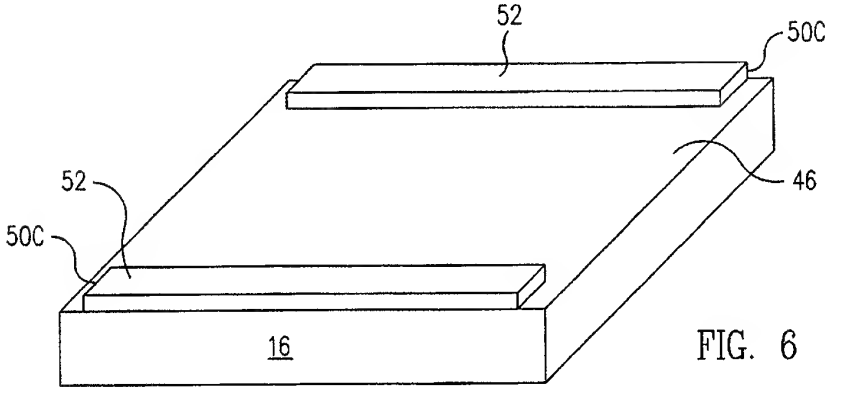


FIG. 6

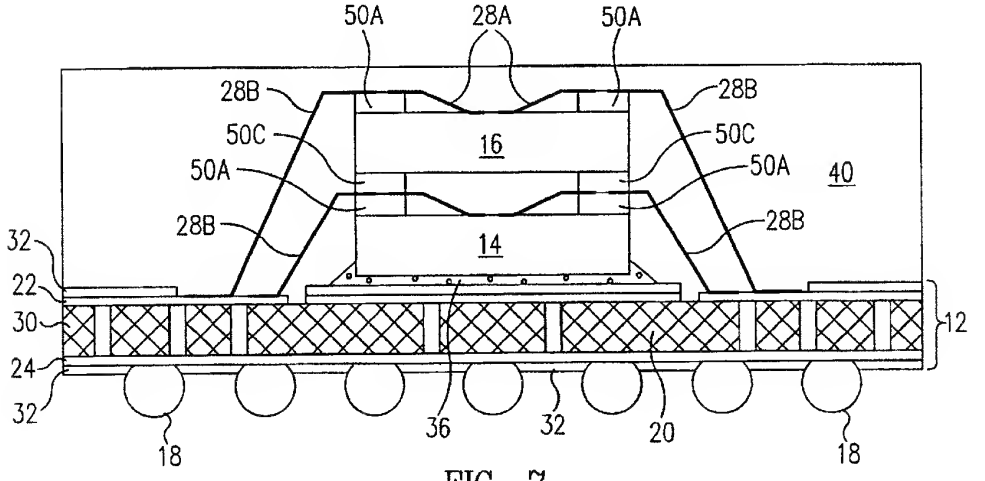


FIG. 7

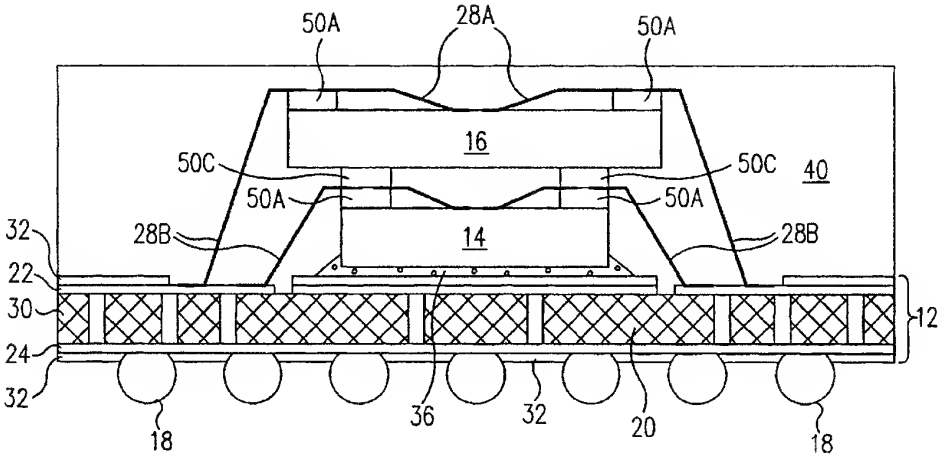

50A
28A
50A
16
50C
50C
40
50A
50A
32
28B
14
28B
22
30
12
24
32
18
36
32
20
18

FIG. 8

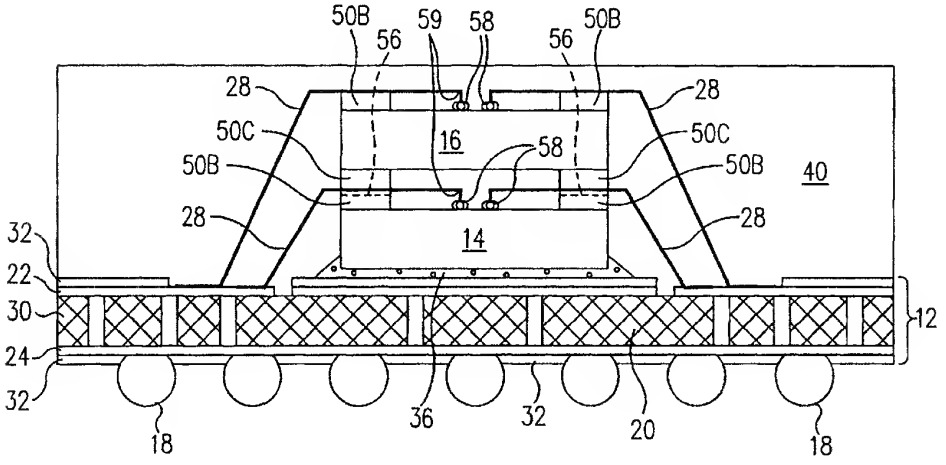

50B
59
58
56
56
50B
28
28
50C
16
58
50C
50B
50B
40
28
28
32
14
22
30
12
24
32
18
36
32
20
18

FIG. 9

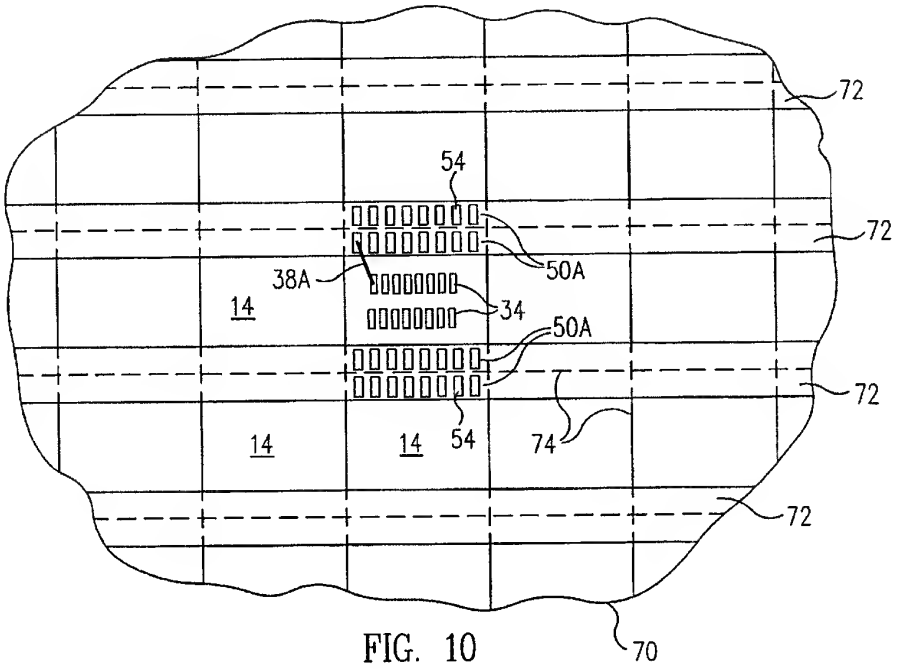

72
54
72
38A
50A
14
34
50A
72
14
14
54
74
72
70

FIG. 10

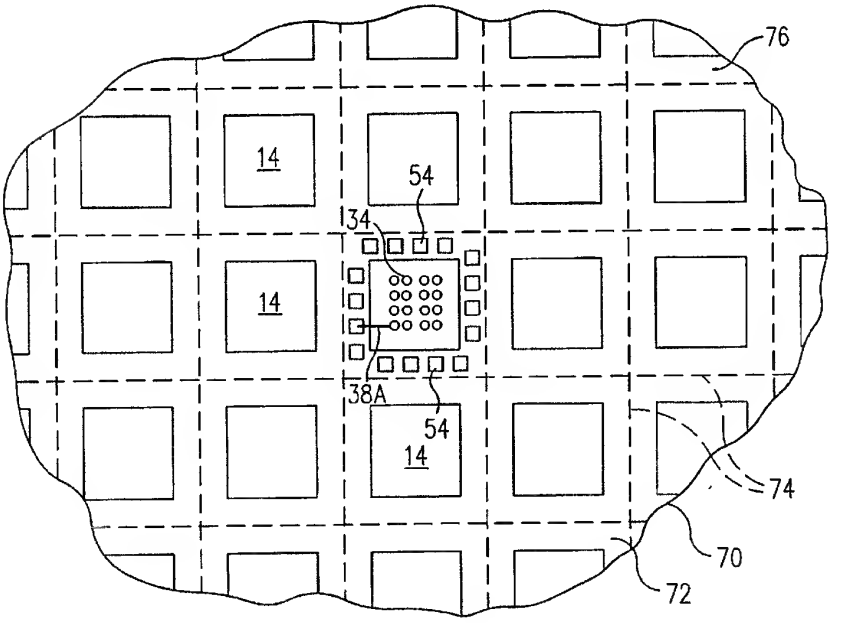

76
14
54
34
14
38A
54
14
74
70
72

FIG. 11

SEMICONDUCTOR PACKAGE WITH SPACER STRIPS

BACKGROUND

1. Field of the Invention

This invention generally relates to semiconductor packages, and in particular, to semiconductor packages having spacer strips that enable one or more semiconductor dies having central terminal pads thereon to be stacked on top of one another and reliably wire bonded to an associated substrate.

2. Description of the Related Art

A typical semiconductor package includes a connective substrate, such as a lead frame or a laminate, that has a semiconductor die, or "microchip," mounted on a surface thereof and electrically connected to the substrate by, e.g., a plurality of fine conductive wires that bond at opposite ends to input/output terminal pads on the tops of the die and the substrate, respectively.

Some dies, such as memory chips, have their terminal pads located in a central portion of the die's active surface, as opposed to at their peripheral edges. Wire bonding of these types of dies can be more problematical because the wires must traverse not only the vertical distance from the edges of the die to the substrate, but also a greater horizontal distance from the edges of the die to the centrally located terminal pads thereon. This increase in the distance traversed by the wires increases the possibility that one or more of the wires may contact the surface of the die and/or each other, and thereby short out. This problem is exacerbated if another die is stacked on top of the first die, as is sometimes done to increase package component density. The problem then becomes one of preventing the wires from shorting to the second die, as well as to the first die and each other.

A need therefore exists in the industry for a semiconductor package incorporating an apparatus that enables one or more semiconductor dies having central terminal pads thereon to be stacked on top of one another in the package and reliably wire bonded to an associated substrate without shorting of the bonding wires to the die(s) and/or each other.

SUMMARY OF THE INVENTION

This invention provides a semiconductor package incorporating "spacer strips" that enable one or more semiconductor dies having central terminal pads to be stacked on top of one another within the package and reliably wire bonded to an associated substrate without shorting of the bonded wires.

The novel package includes a connective substrate having top and bottom surfaces. The bottom surface of a first semiconductor die is attached to the top surface of the substrate. The die has a top surface with a plurality of terminal pads formed on a central portion thereof.

A first pair of spacer strips is mounted on the top surface of the die at its opposite edges such that they straddle the central terminal pads on the die. Each of the spacer strips comprises a flat, elongated strip of an insulative material having a top surface, an opposite bottom surface that is attached to the top surface of the die, and a thickness between the top and bottom surfaces.

The die is electrically connected to the substrate by a plurality of fine conductive wires. In one embodiment, each of the wires has a first end bonded to a corresponding central terminal pad on the die, a second end bonded to a corresponding terminal pad on the first surface of the substrate, and an intermediate portion between the first and second ends that passes transversely across the first surface of a corresponding one of the spacer strips. The spacer strips have spaced transverse grooves in their top surfaces that captivate the intermediate portion of each individual wire, thereby redistributing the wires and isolating them from the die and from each other.

In another embodiment, the spacer strips have spaced bonding pads on their top surfaces. Each of the wires has a first end bonded to a corresponding central terminal pad on the die, a second end bonded to a corresponding terminal pad on the first surface of the substrate, and an intermediate portion between the first and second ends that is bonded to a corresponding one of the bonding pads on a corresponding one of the spacer strips.

In yet another embodiment, the conductive wires comprise associated pairs of wires. A first wire in each pair has a first end bonded to a corresponding terminal pad on the die and a second end bonded to a corresponding bonding pad on a corresponding spacer strip. A second wire in each pair has a first end bonded to a corresponding terminal pad on the substrate and a second end bonded to the same bonding pad on the spacer strip to which the second end of the first wire in the pair is bonded.

A second die can be mounted directly on top of the spacer strips on the first die. Alternatively, a second pair of spacer strips can be mounted on the bottom surface of the second die before it is mounted on top of the first die. Each of the strips in the second pair of spacer strips is positioned in facing opposition to a respective one the strips in the first pair of spacer strips on the first die. The strips cooperate to space the second die above the first die at a controlled distance and prevent the second die from contacting the bonding wires on the first die.

A better understanding of the above and other features and advantages of the present invention may be had from the detailed description below of certain exemplary embodiments thereof, particularly if such consideration is made in conjunction with the several views of the associated drawings.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

FIG. **1** is a top plan view of a semiconductor package incorporating spacer strips in accordance with one exemplary embodiment of the present invention;

FIG. **2** is a cross-sectional, side elevation view of the semiconductor package shown in FIG. **1**, as revealed by the section taken along the lines II—II therein, shown with a single, first die;

FIG. **2A** is a cross-sectional side elevation view of a semiconductor package in accordance with another exemplary embodiment of the present invention;

FIG. **3** is a cross-sectional, side elevation view of the semiconductor package shown in FIG. **1**, shown with a second die stacked on top of the first;

FIG. **4** is an isometric view of a semiconductor die having central terminal pads on its top surface and a pair of spacer strips attached thereto in accordance with another exemplary embodiment of this invention;

FIG. **5** is an isometric view of a semiconductor die having central terminal pads on its top surface and a pair of spacer strips attached thereto in accordance with another exemplary embodiment of this invention;

FIG. 6 is an isometric view of a semiconductor die having a pair of spacer strips attached to its bottom surface in accordance with another exemplary embodiment of this invention;

FIG. 7 is a cross-sectional, side elevation view of a semiconductor package in accordance with another exemplary embodiment this invention;

FIG. 8 is a cross-sectional, side elevation view of a semiconductor package in accordance with another exemplary embodiment this invention;

FIG. 9 is a cross-sectional, side elevation view of a semiconductor package in accordance with another exemplary embodiment this invention;

FIG. 10 is a top plan view of a portion of a semiconductor wafer having spacer strips mounted thereon in accordance with another exemplary embodiment of this invention; and,

FIG. 11 is a pop plan view of a portion of a semiconductor wafer having spacer strips mounted thereon in accordance with another exemplary embodiment of this invention.

DETAILED DESCRIPTION OF THE EXEMPLARY EMBODIMENTS

FIGS. 1, 2 and 3 are a top plan, and two cross-sectional side elevation views, respectively, of a semiconductor package 10 incorporating spacer strips 50A in accordance with two exemplary embodiments of this invention. The packages 10 conventionally include a connective substrate 12 and a first semiconductor die 14 mounted on the top surface of the substrate. In the second, "stacked-die" embodiment illustrated in FIG. 3, a second die 16 has been mounted on top of the first die 14 in the manner described below.

The connective substrate 12 may comprise a flexible resin tape, a rigid fiberglass laminate, a ceramic coupon, or a metal lead frame, all of known types in the industry, depending on the particular type of semiconductor package 10 at hand. The exemplary package 10 illustrated in the figures is a ball grid array ("BGA") type of package, so-called because of the balls of solder 18 formed on the bottom surfaces of the respective substrates 12 that constitute the input/output terminals of the respective packages 10. However, it should be understood that the teachings of this invention are applicable to other types of semiconductor packages having other types of input/output terminals, as well.

The connective substrate 12 illustrated comprises a layer 20 of an insulative material, e.g., a polyimide resin film, laminated between conductive layers 22, 24 of a metal, e.g., copper or aluminum, that comprise the top and bottom surfaces of the substrate, respectively. The conductive layers 22, 24 are typically patterned, e.g., by photolithography techniques, to define terminal pads 26 in the top layer 22 and solder ball lands 28 in the bottom layer 24. The terminal pads 26 are connected to the solder ball lands 28 through the thickness of the insulative layer 20 by vias 30, i.e., plated-through holes in the layers. Either or both of the conductive layers 22, 24 may be coated over with an insulative "solder mask" 32 having openings in it through which the respective terminal pads 26 and solder ball lands 28 are exposed, and which serves to prevent bridging between the pads and/or lands by accidental solder splashes.

The dies 14 and 16 typically include a plurality of input/output terminal pads 34 (see FIGS. 4 and 5) located on their respective top, or "active," surfaces. In some types of dies, typically memory devices, these pads 34 may be located in a central portion of the die, as shown in the plan view of FIGS. 1, 10, and 11, and in the isometric views of FIGS. 4 and 5. During fabrication of the package, the first die 14 is mounted on the substrate 12 by, e.g., a layer of an adhesive 36, such as an epoxy resin.

After the die 14 is mounted to the substrate, it is electrically connected to the substrate 12 by a plurality of fine, conductive wires, typically made of gold or aluminum. Wire bonding is typically effected with automated bonding equipment employing well-known thermal-compression or ultrasonic bonding techniques. After the die 14 is wire bonded to the substrate 12, the die, substrate, and conductive wires are overmolded with a dense, monolithic body 40 (shown dotted in FIGS. 2 and 3) of plastic, typically a filled epoxy resin, to protect the packaged parts from environmental elements, and particularly moisture.

As may be seen in the embodiments illustrated in FIGS. 1–3, because the terminal pads 34 on the top of the first die 14 are located in the central portion of the die, the wires must traverse not only the vertical distance from the edges of the die to the substrate 12, but also the horizontal distance from the edges of the die to the centrally located terminal pads 34. This distance is greater than if the terminal pads 34 were located on the peripheral edges of the die, as they are in other cases, and this greater distance traversed by the wires increases the probability that one or more of them may contact a surface or edge of the die 14 and/or another wire, particularly during the "wire-sweep" that occurs during overmolding of the package body 40, thereby shorting out the wire(s) and resulting in a defective device. This problem is exacerbated in stacked-die structures because of the added possibility that the wires may contact the closely overlying second die 16.

However, it has been discovered that the wire shorting problem can be eliminated simply and inexpensively in both single- and multiple-die types of packages by the provision of one or more pairs of "spacer strips" 50A, 50B, and 50C, such as those illustrated in the figures and described in more detail below.

A first embodiment of the spacer strips 50A is shown in the isometric view of FIG. 4 and as employed in the single- and stacked-die packages 10 illustrated in FIGS. 1–3, and 7 and 8, respectively. A second embodiment of the spacer strips 50B is shown in the isometric view of FIG. 5, and as employed in the stacked-die package 10 configuration illustrated in FIG. 9. A third embodiment of the spacer strips 50C is shown in the isometric view of FIG. 6, and as employed in conjunction with the other spacer strip embodiments 50A and 50B in the stacked die embodiments illustrated in FIGS. 7–9.

Each of the exemplary spacer strips 50A, 50B, and 50C comprises a flat, elongated strip of an insulative material having a first surface 52, and a second surface opposite thereto.

As shown in FIG. 4, the first surface 52 of the first embodiment of spacer strips 50A has a plurality of conductive bonding pads 54 thereon. In use, the second surfaces of a pair of the spacer strips 50A are attached, e.g., with an adhesive, at opposite edges of the top surface of the die 14 such that they straddle the central terminal pads 34 on the die (see FIGS. 1 and 4). The die 14 is then attached to the substrate 12, as above. In the single-die embodiment illustrated in FIG. 2, the conductive bonding wires comprise a first wire 38A having a first end bonded to one of the terminal pads 34 on the die 14 and a second end bonded to a corresponding one of wire bonding pads 52 on a corresponding one of the spacer strips 50A, and a second wire 38B having a first end bonded to a terminal pad 26 on the

substrate **12** and a second end bonded to the corresponding wire bonding pad **54** on the corresponding spacer strip **50**A.

Alternatively, the first and second conductive wires **38**A and **38**B can comprise a single wire **38** having a first end bonded to a terminal pad **34** on the die **12**, a second end bonded to a terminal pad **26** on the substrate **12**, and an intermediate portion **38**C bonded to a corresponding one of the wire bonding pads **54** on a corresponding spacer strip **50**A, as shown in FIG. **2**A.

After the first die **14** is wire honded to the substrate **12**, the second die **16** can he mounted on top of the first die **14**, typically with another layer of an insulative adhesive **44**, for example, a double-hacked adhesive film, to form a "stacked die" structure, as illustrated in FIG. **3**. After the second die **16** is mounted, it is wire bonded to the substrate **12** in a procedure similar to that described above for the first die **14**.

In a variation of the foregoing wire bonding process that is available with the first embodiment of spacer strips **50**A, a pair of the spacer strips **50**A are attached to a die **14** and/or **16**, as above, and the die then "partially" wire bonded, i.e., with only the first one of the wires **38**A, from the central pads **34** on the die to the corresponding bonding pads **54** on the spacer strips **50**A, as illustrated in FIG. **4**. This partial wire bonding of the dies can be effected separately from the rest of the packaging operation, and the partially wire-bonded die-spacer strip assemblies can be cached for later use, at which point they can he treated as conventional dies having wire bonding terminal pads at their edges, instead of their central portions.

As shown in FIG. **5**, the first surface **52** of the second embodiment of spacer strips **50**B has a plurality of transverse grooves **56** in it. In use, the second surfaces of a pair of the second embodiment of spacer strips **50**B are mounted, e.g., with an adhesive, on the top surface of the die **14** at opposite edges thereof such that they straddle the central terminal pads **34** on the die, as in the case of the first embodiment **50**A above.

In the second embodiment, the die **14** is attached to the substrate **12**, as above, and the conductive wires **38** are then bonded, first to a corresponding one of the terminal pads **34** on the die, then down to a corresponding one of the terminal pads **26** on the substrate **12**, or vice-versa, such that, in either case, an intermediate portion of each of the wires **38** is channeled through a corresponding one of the grooves **56** in a corresponding one of the spacer strips **50**B (see FIG. **9**). A similar procedure is followed with respect to the second die **16** after it is attached to the top surface of the first die **14**, as above.

The spacer strips **50**A or **50**B thus serve to captivate the bonding wires **38** and keep them separated from one another and from the surfaces of the dies **14** and **16**, thereby preventing the wires from shorting and resulting in a defective device.

The third embodiment of the spacer strips **50**C can also serve as a convenient agent for the attachment of a second die **16** to the first die **14**, as well as to prevent shorting between the second die and the bonding wires **38**, or **38**A and **38**B on the top of the first die **14**. As illustrated in FIG. **6**, unlike the other two embodiments, the third embodiments of the spacer strips **50**C have a plain, flat, insulative first surface **52**. As shown in FIG. **6**, the third embodiment of spacer strips **50**C is used by mounting the second surfaces of a pair of the strips **50**C on the bottom surface **46** of the second die **16**, e.g., with an adhesive, such that the first surfaces **52** of the spacer strips face away from the die. The strips **50**C may be mounted at the edges of the bottom surface of the die **16**, as shown in FIGS. **6**, **7**, and **9**, or on a larger die, they can be mounted inboard of the die's edges so that they correspond to the positions of a first pair of spacer strips **50**A or **50**B on a smaller, underlying first die **14**, as shown in FIG. **8**.

As shown in each of FIGS. **7**–**9**, the bottom surface **46** of the second die **16** (and, hence, the first surfaces **52** of the second pair of spacer strips **50**C) is then placed over the top surface of the first die **14** such that corresponding pairs of the respective first surfaces **52** of the spacer strips in respective ones of the first and second pairs thereof are in opposed alignment with each other. A portion of each of the conductive wires **38**, or **38**A and **38**B on the first die **14** passes between a corresponding one of the corresponding pairs of opposing first surfaces of the spacer strips and is captivated between them. The second die **16** may then be attached by a layer of adhesive between each of the corresponding pairs of first surfaces **52** of the respective first and second pairs of spacer strips.

As may be seen in FIGS. **7**–**9**, the second pair of spacer strips **50**C on the bottom surface of the second die **16** serve as "standoffs" for the die **16** and prevent the bonding wires **38**, **38**A, **38**B on the first die **14** from shorting to each other and/or the second die.

As an additional benefit, the spacer strips **50**A, **50**B can serve as "spacers" to control the height between the dies of a stacked die package, in the following manner. Those of skill in the packaging art will recognize that, in connection with the bonding of the conductive wires **38**, **38**A, **38**B, the vertical height of wires honded with so-called "hall honds" **58**, such as those shown on the tops of the dies **14** and **16** in FIG. **9**, is greater than that of wires honded with so-called "stitch," "crescent," or "wedge" honds **60**, such as those shown on top of the dies in FIGS. **1**–**8**. This is because a hall-bonded wire **38** departs from the underlying bonding surface perpendicularly, then transitions laterally through a relatively sharp hend **59**, as shown in FIG. **9**, whereas, wires **38**A, **38**B honded with the latter, stitch-type of bonds **60**, which are made with the wire **38**A, **38**B nearly parallel to the honding surface, transition through a much more gradual hend. (Compare, e.g., FIGS. **8** and **9**.)

As a result of the relatively greater height above the die of a wire bonded thereon with a ball bond **58**, extra care must be taken when attaching a second die **16** on the top surface of a first die **14** having ball bonded wires **38** thereon, as shown in FIG. **9**, to accurately control the spacing between the two dies such that the second die does not interfere with or impose undue mechanical stresses on the wires **38**. If corresponding, opposing pairs of spacer strips **50**A or **50**B and **50**C are employed to mount the second die **16** on the first die **14**, as described above, the resulting spacing between the two dies is easily and precisely controlled simply by controlling the thicknesses of the respective spacer strips.

The jumper strips **50**A, **50**B, and **50**C can be made of a variety of insulative materials and hy a variety of techniques. For example, they can be fabricated from a resin tape or a sheet of fiberglass impregnated with an epoxy resin using conventional circuit tape or PCB fabrication techniques.

In other applications, a different insulative material may be more suitable. For example, it will be appreciated that there can be large differences in the respective thermal coefficients of expansion (TCE) of the dies **14**, **16** and the substrate **12**. Thus, the substrate **12**, which may be made of a laminate having a TCE of approximately 15–18 parts-per-million per degree Centigrade (PPM/° C.)), will experience a much greater amount of thermal expansion and contraction

with heating and cooling, respectively, than do the dies **14** and **16**, which are typically made of silicon (TCE=4 PPM/° C.) or other semiconductor material. This difference in their respective amounts of thermal expansion and contraction can impose substantial shear stresses on the respective elements in the package, and particularly the dies, with large temperature excursions.

Thus, in applications intolerant of large thermal stresses, it may he desirahle to fabricate the spacer strips **50A**, **50B**, and **50C** from an insulative material that more closely matches the TCE of the dies **14** and **16**, plus or minus about 2.5 PPM/° C., e.g., a ceramic. For example, the spacer strips **50A** and **50B** can be fabricated from a coupon of silicon oxide, gallium arsenide quartz, alumina, aluminum nitride, or a laminate of the foregoing materials, using conventional semiconductor fabrication techniques and equipment.

In the foregoing exemplary embodiments, the spacer strips **50A**, **50B**, and **50C** are shown and described as deployed in individual pairs mounted on individual dies **14** and **16**. However, it has been discovered that an economy in manufacturing costs can be realized if the spacer strips are fabricated as either elongated strips that are connected tandemly and end-to-end, or in an alternative configuration, as an array of rectangular "frames," that are mounted on the dies before the latter are cut from the parent wafer. This is illustrated in FIGS. **10** and **11**, respectively.

FIG. **10** shows a portion **70** of a semiconductor wafer having a plurality of dies **14** in it. Elongated strips **72**, each having a plurality of spacer strips **50A** connected tandemly and end-to-end with each other, are mounted on the wafer such that they straddle the "streets," or scribe lines **74** in the wafer between the dies **14**. When the dies **14** are separated ("singulated") from the wafer, typically, hy sawing along the scribe lines **74**, hoth the strips **72** and the wafer are cut through simultaneously, and each die is separated with a pair of the spacer strips **50A** already attached to its opposite edges, as shown in FIG. **4**.

A similar arrangement is shown in FIG. **11**, except that in this embodiment, it is desirable to wire bond the dies **14** at all four of their respective edges. In such an embodiment, the jumper strips **50A** may be provided as rectangular frames connected together in an array **76** that is mounted on the wafer before singulation. When the wafer is sawn along the scribe lines **74**, the frames are also cut simultaneously, such that each die **14** is separated with one of the rectangular frames attached to its top surface and centered over the bonding terminals **34** in the central portion of the die.

It will be understood that, in either of the two foregoing exemplary embodiments, the dies **14** can be "partially" wire bonded to their respective spacer strips **50A** with conductive wires **38A** before the dies are singulated from their respective wafers, as described above.

Although the spacer strips **50A**, **50B**, and **50C** of the present invention have been described with reference to certain exemplary embodiments thereof, persons skilled in the art will recognize that many modifications may be made to these in terms of their materials and methods without departing from the spirit and scope of the invention.

In light of the foregoing, it is submitted that the scope of this invention should not be measured by that of the particular embodiments described and illustrated herein, but rather, should encompass that of the claims appended hereafter.

What is claimed is:

1. A semiconductor package, comprising:

a substrate having opposite first and second surfaces;

a first semiconductor die having a first surface with a plurality of terminal pads in a central portion thereof and an opposite second surface mounted on the first surface of the substrate;

a first pair of spacer strips, each comprising a flat, elongated element of an insulative material having a first surface and an opposite second surface mounted on the first surface of the die adjacent to respective opposite edges thereof;

a plurality of electrically conductive paths, each path connecting a terminal pad on the die to a terminal pad on the substrate and having an intermediate portion passing transversely across the first surface of one of the spacer strips;

a means for enclosing the first semiconductor die, the first pair of spacer strips, the electrically conductive paths, and at least a portion of the first surface of the suhstrate within said semiconductor package,

wherein each of the first surfaces of the spacer strips has a plurality of wire bonding pads thereon, and wherein each of the electrically conductive paths comprises

a first metal wire having a first end bonded to one of the terminal pads on the die and a second end bonded to a corresponding one of wire bonding pads; and,

a second metal wire having a first end bonded to a terminal pad on the substrate and a second end bonded to the corresponding wire bonding pad.

2. The semiconductor package of claim **1**, further comprising a second semiconductor die having a first surface and an opposite second surface mounted on the first surfaces of the spacer strips.

3. The semiconductor package of claim **1**, further comprising:

a second semiconductor die having opposite first and second surfaces; and,

a second pair of spacer strips, each comprising a flat, elongated member of an insulative material having a first surface and an opposite second surface mounted on the second surface of the second die,

the second die-being mounted on the first die such that corresponding pairs of respective ones of the first surfaces of respective ones of the spacer strips in respective ones of the first and second pairs of the spacer strips are in opposed alignment with each other, and such that the respective second ends of the metal wires are disposed between a corresponding one of the pairs of opposing first surfaces of the spacer strips.

4. The semiconductor package of claim **3**, wherein the first metal wires are bonded to the terminal pads on the die with hall bonds, and wherein the sum of the thicknesses of the respective spacer strips is equal to or greater than a height of the wires above the die.

5. The semiconductor package of claim **1**, wherein the metal wires are honded to the terminal pads on the die with ball honds, and wherein the sum of the thicknesses of the respective spacer strips is equal to or greater than a height of the wires above the die.

6. A semiconductor package, comprising:

a substrate having opposite first and second surfaces;

a first semiconductor die having a first surface with a plurality of terminal pads in a central portion thereof and an opposite second surface mounted on the first surface of the substrate;

a first pair of spacer strips, each comprising a flat, elongated element of an insulative material having a first surface and an opposite second surface mounted on the first surface of the die adjacent to respective opposite edges thereof;

a plurality of electrically conductive paths, each path connecting a terminal pad on the die to a terminal pad on the substrate and having an intermediate portion passing transversely across the first surface of one of the spacer strips;

a means for enclosing the first semiconductor die, the first pair of spacer strips, the electrically conductive paths, and at least a portion of the first surface of the substrate within said semiconductor package;

a second semiconductor die having opposite first and second surfaces; and,

a second pair of spacer strips, each comprising a flat, elongated member of an insulative material having a first surface and an opposite second surface mounted on the second surface of the second die,

the second die being mounted on the first die such that corresponding pairs of respective ones of the first surfaces of respective ones of the spacer strips in respective ones of the first and second pairs of the spacer strips are in opposed alignment with each other, and such that the intermediate portions of the conductive paths pass between a corresponding one of the pairs of opposing first surfaces of the spacer strips.

7. The semiconductor package of claim **6**, the metal wires are bonded to the terminal pads on the die with ball bonds, and wherein the sum of the thicknesses of the respective spacer strips is equal to or greater than a height of the wires above the die.

8. The semiconductor package of claim **6**, wherein the second semiconductor die includes a first surface with an outer edge, and terminal pad at the first surface; and further comprising:

a second insulative spacer and a second electrically conductive path covered by the means, wherein the second insulative spacer includes a first surface, and an opposite second surface coupled to the first surface of the second semiconductor die between the terminal pad and the outer edge, and the second electrically conductive path passes across the first surface of the second insulative spacer and electrically couples the terminal pad of the second semi-conductor die to the substrate.

9. The semiconductor package of claim **6**, wherein the electrically conductive path comprises a metal wire bonded to the terminal pad on the semiconductor die with a ball bond, and, a thickness of the spacer is equal to or greater than a height of the wire above the die.

10. A semiconductor package comprising:

a substrate;

a semiconductor die coupled to the substrate, said semiconductor die including a first surface with an outer edge, and terminal pad at the first surface;

an insulative spacer having a first surface, and an opposite second surface coupled to the first surface of the semiconductor die between the terminal pad and the outer edge;

an electrically conductive path passing across the first surface of the spacer and electrically coupling the terminal pad to the substrate; and

a means coupled to the substrate for protectively covering the semiconductor die, the spacer, the electrically conductive path, and at least a portion of the substrate,

wherein the spacer includes a groove in the first surface that extends parallel to a direction of the electrically conductive path, and said electrically conductive path passes through said groove.

11. The semiconductor package of claim **10**, wherein the electrically conductive path is a single electrical conductor extending from the terminal pad to the substrate.

12. The semiconductor package of claim **10**, wherein the electrically conductive path comprises a metal wire bonded to the terminal pad on the semiconductor die with a hall bond, and a thickness of the spacer is equal to or greater than a height of the wire above the die.

13. The semiconductor package of claim **10**, further comprising a second semiconductor die within said package over the first semiconductor die, wherein the second semiconductor is coupled to the first surface of the insulative spacer through an insulative layer, and is electrically coupled to the substrate.

14. The semiconductor package of claim **13**, wherein the electrically conductive path is a single electrical conductor extending from the terminal pad to the substrate.

15. A semiconductor package comprising:

a substrate;

a semiconductor die coupled to the substrate, said semiconductor die including a first surface with an outer edge, and terminal pad at the first surface;

an insulative spacer having a first surface, and an opposite second surface coupled to the first surface of the semiconductor die between the terminal pad and the outer edge;

an electrically conductive path passing across the first surface of the spacer and electrically coupling the terminal pad to the substrate; and

a means coupled to the substrate for protectively covering the semiconductor die, the spacer, the electrically conductive path, and at least a portion of the substrate,

wherein the electrically conductive path is a single electrical conductor extending from the terminal pad to the substrate.

16. A semiconductor package comprising:

a substrate;

a semiconductor die coupled to the substrate, said semiconductor die including a first surface with an outer edge, and terminal pad at the first surface;

an insulative spacer having a first surface, an electrically conductive region confined to the first surface of the spacer, and an opposite second surface coupled to the first surface of the semiconductor die between the terminal pad and the outer edge; and

an electrically conductive path passing across the first surface of the spacer and electrically coupling the terminal pad to the substrate, wherein the electrically conductive path includes at least one electrical conductor bonded to the electrically conductive region.

17. The semiconductor package of claim **16**, wherein the electrically conductive path includes a first electrical conductor having a first end coupled to the terminal pad and a second end coupled to the electrically conductive region, and second electrical conductor having a first end coupled to the electrically conductive region and a second end coupled to the substrate.

18. The semiconductor package of claim **16**, further comprising a second semiconductor die over the first semiconductor die.

19. The semiconductor package of claim **18**, further comprising an insulative layer, wherein the second semi-

conductor die is coupled to the first surface of the insulative spacer over the electrically conductive path through the insulative layer.

20. The semiconductor package of claim **18**, wherein the second semiconductor die includes a first surface with an outer edge, and terminal pad at the first surface; and further comprising:

a second insulative spacer and a second electrically conductive path, wherein the second insulative spacer includes a first surface, and an opposite second surface coupled to the first surface of the second semiconductor die between the terminal pad and the outer edge, and the second electrically conductive path passes across the first surface of the second insulative spacer and electrically couples the terminal pad of the second semiconductor die to the substrate.

21. The semiconductor package of claim **16**, wherein the electrically conductive path is a single electrical conductor extending from the terminal pad to the substrate.

22. The semiconductor package of claim **16**, further comprising an enclosure coupled to the substrate and covering the semiconductor die, the spacer, the electrically conductive path, and at least a portion of the substrate.

23. The semiconductor package of claim **16**, wherein the electrically conductive path comprises a metal wire bonded to the terminal pad on the semiconductor die with a ball bond, and a thickness of the spacer is equal to or greater than a height of the wire above the die.

24. The semiconductor package of claim **16**, wherein the electrically conductive path is a single electrical conductor extending from the terminal pad to the substrate.

25. A semiconductor package comprising:

a substrate;

a semiconductor die coupled to the substrate, said semiconductor die including a first surface with a perimeter, and terminal pad at the first surfaee;

an insulative spacer having a first surface, an electrically conductive region confined to the first surface, and a second surface opposite the first surface and coupled to the first surface of the semiconductor die between the terminal pad and the perimeter;

a first electrical conductor coupled between the terminal pad and the electrically conductive region, and a second electrical conductor coupled between the electrically conductive region and the substrate; and

a means coupled to the substrate for protectively covering the semiconductor die, the spacer, the first and second electrical conductors, and at least a portion of the substrate.

26. The semiconductor package of claim **25**, further comprising a second semiconductor die over the first semiconductor die and covered by said means.

27. The semiconductor package of claim **26**, wherein the second semiconductor is coupled to the first surface of the insulative spacer through an insulative layer.

28. The semiconductor package of claim **26**, wherein the second semiconductor die includes a first surface with a perimeter, and terminal pad at the first surface; and

further comprising a second insulative spacer coupled to the first surface of the second semiconductor die between the terminal pad and the perimeter; and

an electrically conductive path passing over the second spacer and electrically coupling the terminal pad of the second semiconductor die and the substrate.

29. A semiconductor package comprising:

a substrate;

a semiconductor die coupled to the substrate, said semiconductor die including a first surface with an outer edge, and terminal pad at the first surface;

an electrically conductive path coupling the terminal pad to the substrate; and

an insulative spacer having a first surface and an opposite second surface, wherein the first surface includes a groove extending parallel to a direction of the electrically conductive path, a portion of the electrically conductive path is within said groove, and the second surface of the insulative spacer is coupled to the first surface of the semiconductor die between the terminal pad and the outer edge.

30. The semiconductor package of claim **29**, further comprising a means coupled to the substrate and for protectively covering the semiconductor die, the spacer, the first and second electrical conductors, and at least a portion of the substrate.

31. The semiconductor package of claim **29**, further comprising an enclosure coupled to the substrate and covering the semiconductor die, the spacer, the electrically conductive path, and at least a portion of the substrate.

32. The semiconductor package of claim **29**, further comprising a second semiconductor die within said package over the first semiconductor die, wherein the second semiconductor is coupled to the first surface of the insulative spacer through an insulative layer, and is electrically coupled to the substrate.

33. The semiconductor package of claim **32**, wherein the electrically conductive path is a single electrical conductor extending from the terminal pad of the first semiconductor die to the substrate.

34. The semiconductor package of claim **32**, wherein the electrically conductive path is a single electrical conductor extending from the terminal pad to the substrate.

35. The semiconductor package of claim **29**, wherein the electrically conductive path is a single electrical conductor extending from the terminal pad to the substrate.

36. A semiconductor package comprising:

a substrate;

a first semiconductor die coupled to the substrate, said first semiconductor die including a first surface with an outer edge, and terminal pad at the first surface;

an insulative spacer having a first surface, and an opposite second surface coupled to the first surface of the first semiconductor die between the terminal pad and the outer edge;

an electrically conductive path passing across the first surface of the spacer and electrically coupling the terminal pad to the substrate; and

a second semiconductor die over the first die and coupled to the first surface of the insulative spacer over the electrically conductive semiconductor path, wherein the second semiconductor die is electrically coupled to the substrate,

wherein the electrically conductive path is a single electrical conductor extending from the terminal pad of the first semiconductor die to the substrate.

37. The semiconductor package of claim **36**, further comprising a means coupled to the substrate and for protectively covering the first and second semiconductor dies, the insulative spacer, the electrically conductive path, and at least a portion of the substrate.

* * * * *

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of species 1 (fig. 3) in the reply filed on 03/24/2005 is acknowledged.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 4, 5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shim et al. (US 6,531,784) in view of Kang et al. (US 2003/017810 A1).

4. Regarding claim 1, Shim (e.g. figs. 9 & 5) shows a die containing package comprising: a die 14 defining electrical die contacts 34, the die contacts arranged along a first and an opposite side of the die (i.e. left side from the geometrical center line and right side from the geometrical center line of the chip), a substrate 30 defining first substrate contacts 22, flattened electrical conductive balls 58 attached to the die contacts and making electrical connection thereto, electrical conductive runs 24 on the substrate that run substantially under the die connecting the first substrate contacts, wherein the first substrate contacts are located adjacent to the first side of the die, to second substrate contacts 22, wherein the second substrate contacts are located adjacent to the opposite side of the die, electrically conductive wires 28 with first ends making electrical connections to the first substrate contacts, wherein the wires are

formed to run substantially parallel to the surface of the die, and wherein the other ends are horizontally attached to the flattened balls.

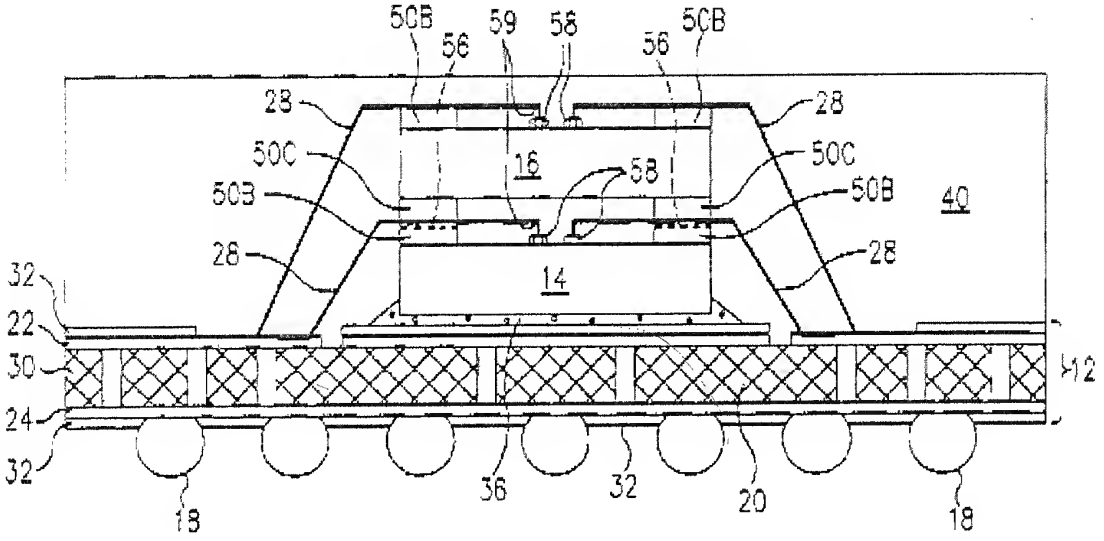
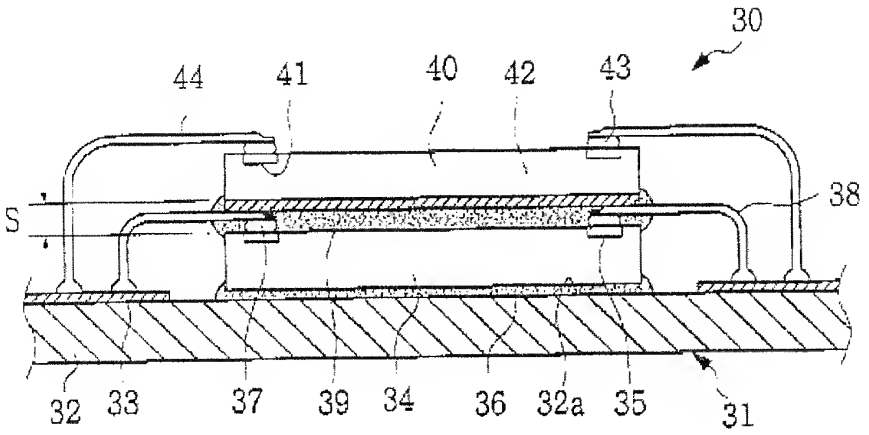


FIG. 9

Shim does not teach that other ends are horizontally attached to the flattened ball. Nevertheless, Kang (e.g. fig. 3) shows electrically conductive wires 38 that run substantially parallel to the surface of the die and have ends that are horizontally attached to flattened balls 37. According to Kang, this type of connection minimizes a space between the first chip and a second chip, thereby reducing the total height of the semiconductor stack (abstract).



It would have been obvious to one of ordinary skill in the art at the time the invention was made to horizontally attach the other ends of the wires disclosed by Shim to the fattened balls in accordance to Kang's invention to minimize the space between the first and the second chip, thereby reducing the total height of the semiconductor stack.

5. Regarding claim 4, Shim shows that the second substrate contacts are located to accommodate a pin out different from the die.

6. Regarding claim 5, Shim (e.g. fig. 9) shows process for packaging a die comprising the steps of: defining electrical die contacts, the electrical die contacts arranged along a first and an opposite side of the die (i.e. left side from the geometrical center line and right side from the geometrical center line of the chip), defining a substrate 12 with first substrate contacts 22, flattening an electrical conductive balls 58, attaching the flattened electrically conductive balls to the die contacts, forming electrical conductive runs 22/24 on the substrate 12 that run substantially under the die connecting the first substrate contacts, wherein the first substrate contacts are located

adjacent to the first side of the die, to second substrate contacts 22 wherein the second substrate contacts are located adjacent to the opposite side of the die, connecting electrically conductive wires 28 to the first substrate contacts, running the electrically conductive wires substantially parallel to the surface of the die contacts and attaching the other ends of the wires to the flattened electrically conductive balls thereby making electrical connections therebetween and wherein the other ends remain substantially parallel to the surface of the die. Shim does not teach that other ends are horizontally attached to the flattened ball. Nevertheless, Kang (e.g. fig. 3) shows electrically conductive wires 38 that run substantially parallel to the surface of the die and have ends that are horizontally attached to flattened balls 37. According to Kang, this type of connection minimizes a space between the first chip and a second chip, thereby reducing the total height of the semiconductor stack (abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to horizontally attach the other ends of the wires disclosed by Shim to the fattened balls in accordance to Kang's invention to minimize the space between the first and the second chip, thereby reducing the total height of the semiconductor stack.

7. Regarding claim 8, Shim shows that the second substrate contacts are located to accommodate a pin out 18 different from the die.

Response to Arguments

8. Applicant's arguments filed 5/22/2007 have been fully considered but they are not persuasive.

9. Applicant argues that the prior art does not show "electrical conductive runs on the substrate that run substantially under the die connecting the first substrate contacts". Nonetheless, Shim (e.g. fig. 9) shows electrical conductive runs 24 on the substrate that run substantially under the die connecting the first and second substrate contacts 22. Note that the contacts 22 are connected by vias or plated holes. Arguments of counsel cannot take the place of factually supported objective evidence. See, e.g., *In re Huang, 100 F.3d 135,139-40, 40 USPQ2d 1685, 1689 (Fed. Cir. 1996); In re De Blauwe, 736 F.2d 699, 705, 222 USPQ 191, 196 (Fed. Cir. 1984).*

10. In response to applicant's argument that "runner under the die provides the advantage of allowing a die- up die to be packaged in a die-down package. It provides the side to side reversal of the contacts so that the die contacts match those of the package regardless of the "die-up" or "die-down" types", the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonardo Andújar whose telephone number is 571-272-1912. The examiner can normally be reached on Mon through Thu from 9:00 AM to 7:30 PM EST.

13. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

14. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Leonardo Andújar

Primary Examiner
Art Unit 2826

7/30/2007